CLAIMS

1. A memory manager for use in connection with a memory, the memory manager comprising:

A. a memory access request receiver module configured to receive an access request requesting an access operation in connection with the memory, the access request including an address;

B. an address translation module configured to,

(i) if the access request requests an access operation in connection with one of a plurality of sections of the memory, provide the address in the access request as an absolute address identifying at least one storage location in the one section; and

(ii) if the access request requests an access operation in connection with another of said sections, generate an absolute address from the address provided in the access request, the address in the access request including a segment identifier and an offset, the address translation module being configured to process the segment identifier and offset to generate an absolute address identifying at least one storage location in the other of said sections; and

C. a memory access operation control module configured to perform an access operation in connection with the memory using the absolute address generated by the address translation module.

2. A memory manager as defined in claim 1 in which each of the segment identifier and offset comprises a plurality of digits arranged in respective ones of a plurality of digit positions, the address translation module being configured to, if the access request requests an access operation in connection with said another of said sections, generate the absolute address by shifting the digits comprising the segment identifier to higher-order digit positions thereby to provide a shifted segment identifier, and adding the offset to the shifted segment identifier.

3. A memory manager as defined in claim 1 in which the segment identifier identifies a segment in said another of said sections, the segment comprising a selected number of storage locations, the address translation module being further configured to perform a verification operation in connection with the offset to verify that the offset identifies a storage location in the segment identified by the segment identifier.

4. A memory manager as defined in claim 3 in which said another of said sections operates as a cache memory, at least one of said segments comprising a cache slot.

5. A memory manager as defined in claim 4 in which the memory further comprises yet another section for which, if the access request requests an access operation in connection therewith, the address translation module is configured to generate an absolute address from the address provided in the access request, the address in the access request including a segment identifier and an offset, the address translation module being configured to process the segment identifier and offset to generate an absolute address identifying at least one storage location in the yet another of said sections, the yet another section comprising a directory for the cache memory.

6. A memory management method for use in managing a memory, the memory management method comprising the steps of:

A. receiving an access request requesting an access operation in connection with the memory, the access request including an address;

B. an address translation step in which,

(i) if the access request requests an access operation in connection with one of a plurality of sections of the memory, the address in the access request is provided as an absolute address identifying at least one storage location in the one section; and

(ii) if the access request requests an access operation in connection with another of said sections, an absolute address is generated from the address provided in the access request, the address in the access request including a segment identifier and an offset, the address translation module being configured to process the segment identifier and offset to generate an absolute address identifying at least one storage location in the other of said sections; and

C. memory access operation control step in which an access operation is performed in connection with the memory using the absolute address generated during the address translation step.

7. A memory management method as defined in claim 6 in which each of the segment identifier and offset comprises a plurality of digits arranged in respective ones of a plurality of digit positions, the address translation step including the step of, if the access request requests an access operation in connection with said another of said sections, generating the absolute address by shifting the digits comprising the segment identifier to higher-order digit positions thereby to provide a shifted segment identifier, and adding the offset to the shifted segment identifier.

8. A memory management method as defined in claim 6 in which the segment identifier identifies a segment in said another of said sections, the segment comprising a selected number of storage locations, the address translation step including the step of performing a verification operation in connection with the offset to verify that the offset identifies a storage location in the segment identified by the segment identifier.

9. A memory management method as defined in claim 8 in which said another of said sections operates as a cache memory, at least one of said segments comprising a cache slot.

10. A memory management method as defined in claim 9 in which the memory further comprises yet another section for which, if the access request requests an access operation in connection therewith, the address translation step includes the step of generating an absolute address from the address provided in the access request, the address in the access request including a segment identifier and an offset, the address translation step including the step of processing the segment identifier and offset to generate an absolute address identifying at least one storage location in the yet another of said sections, the yet another section comprising a directory for the cache memory.

11. A computer program product for use in connection with a digital data processor to provide memory manager for use in connection with a memory, the computer program product comprising a machine readable medium having encoded thereon:

A. a memory access request receiver module configured to enable the processor to receive an access request requesting an access operation in connection with the memory, the access request including an address;

B. an address translation module configured to enable the processor to,

(i) if the access request requests an access operation in connection with one of a plurality of sections of the memory, provide the address in the access request as an absolute address identifying at least one storage location in the one section; and

(ii) if the access request requests an access operation in connection with another of said sections, generate an absolute address from the address provided in the access

request, the address in the access request including a segment identifier and an offset, the address translation module being configured to enable the processor to process the segment identifier and offset to generate an absolute address identifying at least one storage location in the other of said sections; and

C. a memory access operation control module configured to enable the processor to perform an access request in connection with the memory using the absolute address generated by the address translation module.

12. A computer program product as defined in claim 11 in which each of the segment identifier and offset comprises a plurality of digits arranged in respective ones of a plurality of digit positions, the address translation module being configured to enable the processor to, if the access request requests an access operation in connection with said another of said sections, generate the absolute address by shifting the digits comprising the segment identifier to higher-order digit positions thereby to provide a shifted segment identifier, and adding the offset to the shifted segment identifier.

13. A computer program product as defined in claim 11 in which the segment identifier identifies a segment in said another of said sections, the segment comprising a selected number of storage locations, the address translation module being further configured to enable the processor to perform a verification operation in connection with the offset to verify that the offset identifies a storage location in the segment identified by the segment identifier.

14. A computer program product as defined in claim 13 in which said another of said sections operates as a cache memory, at least one of said segments comprising a cache slot.

15. A computer program product as defined in claim 14 in which the memory further comprises yet another section for which, if the access request requests an access operation in connection therewith, the address translation module is configured to enable the processor to generate an absolute address from the address provided in the access request, the address in the access request including a segment identifier and an offset, the address translation module being configured to enable the processor to process the segment identifier and offset to generate an absolute address identifying at least one storage location in the yet another of said sections, the yet another section comprising a directory for the cache memory.